Electronic Version
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Claims

[c1] 1. A flip-chip package substrate, on which a chip shaped as a rectangle is suited to be disposed and to which the chip is suited to be electrically connected, the chip comprising two first opposite sides opposite to each other, two second opposite sides opposite to each other, a first centerline, and a second centerline, the first centerline perpendicularly and evenly dividing the first two opposite sides, the second centerline perpendicularly and evenly dividing the second two opposite sides, the substrate comprising:

a plurality of electrically conductive layers sequentially stacked with each other;

a plurality of isolation layers disposed between two neighboring layers of the electrically conductive layers respectively to electrically isolate the electrically conductive layers; and

a plurality of via-hole traces penetrating at least one layer of the isolation layers to electrically connect at least two layers of the electrically conductive layers,

wherein the substrate comprises a first surface and a corresponding second surface, the chip is adapted to be disposed on the first surface of the substrate, the sub-

strate further comprises a core connection-pad layout region and a peripheral connection-pad layout region, both of them are disposed on the second surface of the substrate, the peripheral connection-pad layout region surrounds the core connection-pad layout region, and the peripheral connection-pad layout region comprises a first centerline neighboring region, a second centerline neighboring region, a third centerline neighboring region and a fourth centerline neighboring region, the first centerline neighboring region and the second centerline neighboring region are disposed on the substrate at two opposite sides of the chip, the third centerline neighboring region and the fourth centerline neighboring region are disposed on the substrate at the other two opposite sides of the chip, the first centerline traverses the first centerline neighboring region and the second centerline neighboring region, the second centerline traverses the third centerline neighboring region and the fourth centerline neighboring region, the second surface of the substrate comprises a plurality of common padable areas, a plurality of first central padable areas, a plurality of second central padable areas, a plurality of third central padable areas and a plurality of fourth central padable areas, part of the common padable areas are disposed in the core connection-pad layout region, the other part of the common padable areas are disposed in

the peripheral connection-pad layout region and far away from the first centerline and the second centerline, the first central padable areas are disposed in the first centerline neighboring region, the second central padable areas are disposed in the second centerline neighboring region, the third central padable areas are disposed in the third centerline neighboring region, and the fourth central padable areas are disposed in the fourth centerline neighboring region,

within the first centerline neighboring region, at both sides of the first centerline is respectively lined with the first central padable areas in three rows, the first central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses between the first central padable areas arranged in two neighboring rows, and the ratio of the number of the first central padable areas with the connection pads for transmitting signals to the total number of the first central padable areas is either equal to or less than 2/7.

[c2] 2. The flip-chip package substrate of claim 1, wherein within the second centerline neighboring region, at both sides of the first centerline is respectively lined with the second central padable areas in three rows, the second central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses between

the second central padable areas arranged in two neighboring rows, and the ratio of the number of the second central padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is either equal to or less than 2/7.

[c3] 3. The flip-chip package substrate of claim 1, wherein within the second centerline neighboring region is lined with the second central padable areas in five rows, the second central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses the second central padable areas arranged in a central row, and the ratio of the number of the second central padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is either equal to or less than 2/7.

[c4] 4. The flip-chip package substrate of claim 1, wherein within the third centerline neighboring region, at both sides of the second centerline is respectively lined with the third central padable areas in three rows, the third central padable areas in each row are lined in parallel to the second centerline, and the second centerline traverses between the third central padable areas arranged in two neighboring rows, the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third cen-

tral padable areas is either equal to or less than 2/7.

[c5] 5. The flip-chip package substrate of claim 1, wherein within the third centerline neighboring region is lined with the third central padable areas in five rows, the third central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses the third central padable areas arranged in a central row, the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third central padable areas is either equal to or less than 2/7.

[c6] 6. The flip-chip package substrate of claim 1, wherein within the second centerline neighboring region, at both sides of the first centerline is respectively lined with the second central padable areas in three rows, the second central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses between the second central padable areas arranged in two neighboring rows, the ratio of the number of the second central padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is either equal to or less than 2/7, within the third centerline neighboring region, at both sides of the second centerline is respectively lined with the third central padable areas in three rows, the third central

padable areas in each row are lined in parallel to the second centerline, the second centerline traverses between the third central padable areas arranged in two neighboring rows, the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third central padable areas is either equal to or less than 2/7, within the fourth centerline neighboring region, at both sides of the second centerline is respectively lined with the fourth central padable areas in three rows, the fourth central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses between the fourth central padable areas arranged in two neighboring rows, and the ratio of the number of the fourth central padable areas with the connection pads for transmitting signals to the total number of the fourth central padable areas is either equal to or less than 2/7.

[c7] 7. The flip-chip package substrate of claim 1, wherein within the second centerline neighboring region, at both sides of the first centerline is respectively lined with the second central padable areas in three rows, the second central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses between the second central padable areas arranged in two neighboring rows, the ratio of the number of the second cen-

tral padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is either equal to or less than 2/7, within the third centerline neighboring region is lined with the third central padable areas in five rows, the third central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses the third central padable areas arranged in a central row, the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third central padable areas is either equal to or less than 2/7, within the fourth centerline neighboring region is lined with the fourth central padable areas in five rows, the fourth central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses the fourth central padable areas arranged in a central row, and the ratio of the number of the fourth central padable areas with the connection pads for transmitting signals to the total number of the fourth central padable areas is either equal to or less than 2/7.

[c8] 8. The flip-chip package substrate of claim 1, wherein the core connection-pad layout region is contiguous to the peripheral connection-pad layout region.

[c9] 9. The flip-chip package substrate of claim 1, wherein the core connection-pad layout region is apart from the peripheral connection-pad layout region in a certain distance.

[c10] 10. The flip-chip package substrate of claim 1, wherein all of the first central padable areas are defined by a plurality of connection pads of the substrate.

[c11] 11. The flip-chip package substrate of claim 1, wherein there are no connection pads at one or more of the first central padable areas.

[c12] 12. A flip-chip package substrate, on which a chip shaped as a rectangle is suited to be disposed and to which the chip is suited to be electrically connected, the chip comprising two first opposite sides opposite to each other, two second opposite sides opposite to each other, a first centerline, and a second centerline, the first centerline perpendicularly and evenly dividing the first two opposite sides, the second centerline perpendicularly and evenly dividing the second two opposite sides, the substrate comprising:
a plurality of electrically conductive layers sequentially stacked with each other;
a plurality of isolation layers disposed between two neighboring layers of the electrically conductive layers

respectively to electrically isolate the electrically conductive layers; and

a plurality of via-hole traces penetrating at least one layer of the isolation layers to electrically connect at least two layers of the electrically conductive layers,

wherein the substrate comprises a first surface and a corresponding second surface, the chip is adapted to be disposed on the first surface of the substrate, the substrate further comprises a core connection-pad layout region and a peripheral connection-pad layout region, both of them are disposed on the second surface of the substrate, the peripheral connection-pad layout region surrounds the core connection-pad layout region, and the peripheral connection-pad layout region comprises a first centerline neighboring region, a second centerline neighboring region, a third centerline neighboring region and a fourth centerline neighboring region, the first centerline neighboring region and the second centerline neighboring region are disposed on the substrate at two opposite sides of the chip, the third centerline neighboring region and the fourth centerline neighboring region are disposed on the substrate at the other two opposite sides of the chip, the first centerline traverses the first centerline neighboring region and the second centerline neighboring region, the second centerline traverses the third centerline neighboring region and the fourth cen-

terline neighboring region, the electrically conductive layer nearest to the second surface of the substrate comprises a plurality of common padable areas, a plurality of first central padable areas, a plurality of second central padable areas, a plurality of third central padable areas and a plurality of fourth central padable areas, part of the common padable areas are disposed in the core connection-pad layout region, the other part of the common padable areas are disposed in the peripheral connection-pad layout region and far away from the first centerline and the second centerline, the first central padable areas are disposed in the first centerline neighboring region, the second central padable areas are disposed in the second centerline neighboring region, the third central padable areas are disposed in the third centerline neighboring region, and the fourth central padable areas are disposed in the fourth centerline neighboring region,

within the first centerline neighboring region is lined with the first central padable areas in five rows, the first central padable areas are lined in parallel to the first centerline, the first centerline traverses the first central padable areas arranged in a central row, and the ratio of the number of the first central padable areas with the connection pads for transmitting signals to the total number of the first central padable areas is either equal

to or less than 2/7.

[c13] 13. The flip-chip package substrate of claim 12, within the second centerline neighboring region are lined with the second central padable areas in five rows, the second central padable areas in each row are lined in parallel to the first centerline, and the first centerline traverses the second central padable areas arranged in a central row, and the ratio of the number of the second central padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is either equal to or less than 2/7.

[c14] 14. The flip-chip package substrate of claim 12, within the third centerline neighboring region is lined with the second central padable areas in five rows, the third central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses the third central padable areas arranged in a central row, and the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third central padable areas is either equal to or less than 2/7.

[c15] 15. The flip-chip package substrate of claim 12, within the second centerline neighboring region is lined with the second central padable areas in five rows, the second

central padable areas in each row are lined in parallel to the first centerline, the first centerline traverses the second central padable areas arranged in a central row, the ratio of the number of the second central padable areas with the connection pads for transmitting signals to the total number of the second central padable areas is less than 2/7, within the third centerline neighboring region is lined with the third central padable areas in five rows, the third central padable areas are lined in parallel to the second centerline, the second centerline traverses the third central padable areas arranged in a central row, the ratio of the number of the third central padable areas with the connection pads for transmitting signals to the total number of the third central padable areas is either equal to or less than 2/7, within the fourth centerline neighboring region is lined with the fourth central padable areas in five rows, the fourth central padable areas in each row are lined in parallel to the second centerline, the second centerline traverses the fourth central padable areas arranged in a central row, and the ratio of the number of the fourth central padable areas with the connection pads for transmitting signals to the total number of the fourth central padable areas is either equal to or less than 2/7.

[c16] 16. The flip-chip package substrate of claim 12, wherein

the core connection-pad layout region is contiguous to the peripheral connection-pad layout region.

[c17] 17. The flip-chip package substrate of claim 12, wherein the core connection-pad layout region is apart from the peripheral connection-pad layout region in a certain distance.

[c18] 18. The flip-chip package substrate of claim 12, wherein all of the first central padable areas are defined by a plurality of connection pads of the substrate.

[c19] 19. The flip-chip package substrate of claim 12, wherein there are no connection pads at one or more of the first central padable areas.

[c20] 20. A flip-chip package substrate having a first surface and a corresponding second surface, a chip adapted to be disposed on the first surface of the substrate and to be electrically connected to the substrate, the chip having a centerline evenly dividing the chip, the substrate further having a peripheral connection-pad layout region disposed on the second surface, the peripheral connection-pad layout region having a centerline neighboring region which the centerline traverses, the substrate comprising:

a plurality of central padable areas disposed in the cen-

terline neighboring region, wherein within the centerline neighboring region, at both sides of the centerline are respectively lined with the central padable areas in three rows, the central padable areas in each row are lined in parallel to the centerline, and the centerline traverses between the central padable areas arranged in two neighboring rows, and the ratio of the number of the central padable areas with the connection pads for transmitting signals to the total number of the central padable areas is either equal to or less than 2/7.

[c21] 21. The flip-chip package substrate of claim 20, wherein all of the central padable areas are defined by a plurality of connection pads of the substrate.

[c22] 22. The flip-chip package substrate of claim 20, wherein there are no connection pads at one or more of the central padable areas.

[c23] 23. A flip-chip package substrate having a first surface and a corresponding second surface, a chip adapted to be disposed on the first surface of the substrate and to be electrically connected to the substrate, the chip having a centerline evenly dividing the chip, the substrate further having a peripheral connection-pad layout region disposed on the second surface, the peripheral connection-pad layout region having a centerline neighboring

region which the centerline traverses, the substrate comprising:

a plurality of central padable areas disposed in the centerline neighboring region, wherein within the centerline neighboring region is lined with the central padable areas in five rows, the central padable areas in each row are lined in parallel to the centerline, the centerline traverses the central padable areas arranged in a central row, and the ratio of the number of the central padable areas with the connection pads for transmitting signals to the total number of the central padable areas is either equal to or less than 2/7.

[c24] 24. The flip-chip package substrate of claim 23, wherein all of the central padable areas are defined by a plurality of connection pads of the substrate.

[c25] 25. The flip-chip package substrate of claim 23, wherein there are no connection pads at one or more of the central padable areas.